ABSTRACT OF THE DISCLOSURE

Inwardly-tapered openings are created in an Anti-Reflection Coating layer (ARC layer) provided beneath a patterned photoresist layer. The smaller, bottom width dimensions of the inwardly-tapered openings are used for defining further openings in an interlayer dielectric region (ILD) provided beneath the ARC layer. In one embodiment, the ILD separates an active layers set of an integrated circuit from its first major interconnect layer. Further in one embodiment, a taper-inducing etch recipe is used to create the inwardly-tapered ARC openings, where the etch recipe uses a mixture of CF4 and CHF3 and where the CF4/CHF3 volumetric inflow ratio is substantially less than 5 to 1, and more preferably closer to 1 to 1.

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